ABSTRACT OF THE DISCLOSURE

In a substrate vertical transistor cells are formed and are arranged, in a transistor cell array, row by row in an x direction and column by column in a y direction. Lower source/drain regions of the transistor cells are connected to a common connection plate. Upper source/drain regions of the transistor cells impart a contact connection for instance to a storage capacitor of a DRAM memory cell. Active trenches running between the transistor cells with word lines are formed along the x direction. The word lines form gate electrodes in sections. A potential at the gate electrode controls a conductive channel in an active region arranged in each case between the upper and the lower source/drain connection region. According to the invention, the active regions of adjacent transistor cells are sections of a contiguous layer body and are connected to one another. An accumulation of charge carriers in the active region and floating body effects are avoided without increasing the area requirement of a transistor cell.